Radiation Hardened, SEE Hardened, Non-Inverting, Quad CMOS Driver

ISL7457SRH

The ISL7457SRH is a radiation hardened, SEE hardened, high speed, non-inverting, quad CMOS driver. It is capable of running at clock rates up to 40MHz and features 2A typical peak drive capability and a nominal On-resistance of just 3.5Ω. The ISL7457SRH is ideal for driving highly capacitive loads, such as storage and vertical clocks in CCD applications. It is also well suited to level-shifting and clock-driving applications.

Each output of the ISL7457SRH can be switched to either the high (V_H) or low (V_L) supply pins, depending on the related input pin. The inputs are compatible with both 3.3V and 5V CMOS logic. The output enable (OE) pin can be used to put the outputs into a high-impedance state. This is especially useful in CCD applications, where the driver should be disabled during power-down.

The ISL7457SRH also features very fast rise and fall times, which are typically matched to within 1ns. The propagation delay is also matched between rising and falling edges to typically within 1.5ns.

The ISL7457SRH is available in a 16 Ld ceramic flatpack package and specified for operation over the full -55°C to +125°C ambient temperature range.

Related Literature

- AN1458, Extending the TID Capability of the ISL7457SRH

Applications

- CCD Drivers, Clock/line Drivers, Level-Shifters

Features

- Electrically screened to SMD 5962-08230
- QML qualified per MIL-PRF-38535 requirements
- Full mil-temp range operation . . . . . T_A = -55°C to +125°C
- Radiation hardness
  - TID [50-300 rad(Si)/s] . . . . . .10krad(Si) min
- SEE hardness
  - LET (SEL and SEB Immunity) . . . . . 40MeV/mg/cm^2 min
  - LET [SET = ΔV_{OUT} < 15V, Δt < 500ns] . . . 40MeV/mg/cm^2
- 4 Channels
- Clocking speeds up to 40MHz
- 11ns/12ns typical t_R/t_F with 1nF Load (15V bias)
- 1ns typical rise and fall time match (15V bias)
- 1.5ns typical prop delay match (15V bias)
- Low quiescent current - < 1mA Typical
- Fast output enable function - 12ns typical (15V bias)
- Wide output voltage range
  - 0V ≤ V_L ≤ 8V
  - 2.5V ≤ V_H ≤ 16.5V
- 2A typical peak drive current (15V Bias)
- 3.5Ω typical on-resistance (15V bias)
- Input level shifters
- 3.3V/5V CMOS compatible inputs

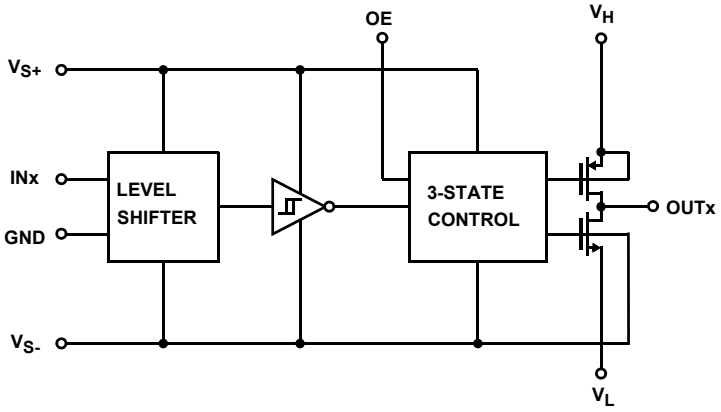


FIGURE 1. BLOCK DIAGRAM

Ordering Information

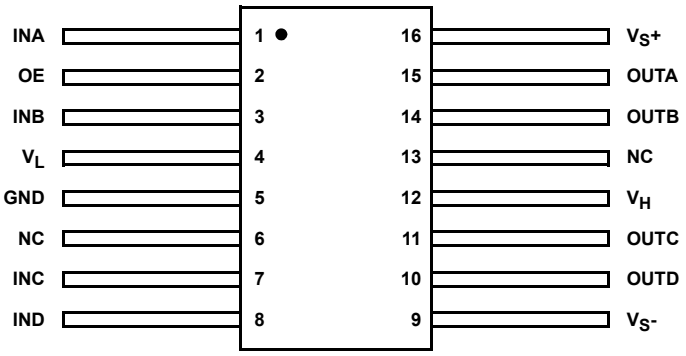
ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962D0823001QXC	ISL7457SRHQF	-55 to +125	16 Ld Flatpack	k16.A
5962D0823001VXC	ISL7457SRHVF	-55 to +125	16 Ld Flatpack	k16.A
5962D0823001V9A	ISL7457SRHVX	-55 to +125	Die	
ISL7457SRHF/PROTO	ISL7457SRHF/PROTO	-55 to +125	16 Ld Flatpack	k16.A
ISL7457SRHX/SAMPLE	ISL7457SRHX/SAMPLE	-55 to +125	Die	

NOTES:

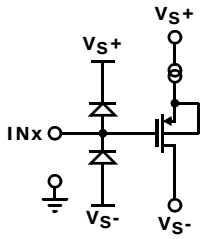
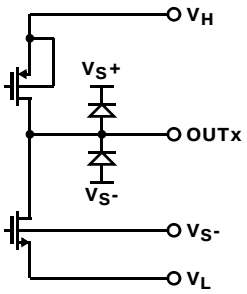
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.
2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pin Configuration

ISL7457SRH
(16 LD FLATPACK)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	INA	Input Channel A	 CIRCUIT 1
2	OE	Output enable	(Reference Circuit 1)
3	INB	Input Channel B	(Reference Circuit 1)
4	V_L	Low voltage input pin	
5	GND	Input logic ground	
6, 13	NC	No connection	
7	INC	Input Channel C	(Reference Circuit 1)
8	IND	Input Channel D	(Reference Circuit 1)
9	V_S-	Negative supply voltage	
10	OUTD	Output Channel D	 CIRCUIT 2
11	OUTC	Output Channel C	(Reference Circuit 2)
12	V_H	High voltage input pin	
14	OUTB	Output Channel B	(Reference Circuit 2)
15	OUTA	Output Channel A	(Reference Circuit 2)
16	V_S+	Positive supply voltage	

Electrical Specifications

Typical values reflect $V_S+ = V_H = 5V$, $V_S- = V_L = 0V$, $OE = V_S+$, $T_A = +25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{IH}	Logic “1” Input Voltage			1.3		V
I_{IH}	Logic “1” Input Current	INx = V_S+		10		nA
V_{IL}	Logic “0” Input Voltage			1.23		V
I_{IL}	Logic “0” Input Current	INx = 0V		-5		nA
C_{IN}	Input Capacitance			5.7		pF
R_{IN}	Input Resistance			500		MΩ
OUTPUT						
R_{OH}	ON-Resistance V_H to OUTx	INx = V_S+, I_{OUTx} = -100mA		8		Ω
R_{OL}	ON-Resistance V_L to OUTx	INx = 0V, I_{OUTx} = +100mA		6		Ω
I_{LEAK+}	Positive Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S+		5		nA
I_{LEAK-}	Negative Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S-		-5		nA
POWER SUPPLY						
I_{S+}	V_S+ Supply Current	INx = 0V and V_S+		0.2		mA
I_{S-}	V_S- Supply Current	INx = 0V and V_S+		-0.2		mA
I_H	V_H Supply Current	INx = 0V and V_S+		0.1		µA
I_L	V_L Supply Current	INx = 0V and V_S+		0.1		µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	INx = 0V to 4.5V step, C_L = 1nF		23		ns
t_F	Fall Time	INx = 4.5V to 0V step, C_L = 1nF		20		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 1nF		3		ns
t_D+	Turn-On Delay Time	INx = 0V to 4.5V step, C_L = 1nF		20		ns
t_D-	Turn-Off Delay Time	INx = 4.5V to 0V step, C_L = 1nF		22		ns
t_{DD}	t_D+, t_D- Mismatch	C_L = 1nF		2		ns
t_{ENABLE}	Enable Delay Time	INx = V_S+, OE = 0V to 4.5V step, R_L = 1kΩ		21		ns
$t_{DISABLE}$	Disable Delay Time	INx = V_S+, OE = 4.5V to 0V step, R_L = 1kΩ		46		ns

Electrical Specifications

Typical values reflect $V_S+ = V_H = 15V$, $V_S- = V_L = 0V$, $OE = V_S+$, $T_A = +25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{IH}	Logic “1” Input Voltage			1.63		V
I_{IH}	Logic “1” Input Current	INx = V_S+		10		nA
V_{IL}	Logic “0” Input Voltage			1.4		V
I_{IL}	Logic “0” Input Current	INx = 0V		-5		nA
C_{IN}	Input Capacitance			5.7		pF
R_{IN}	Input Resistance			1.5		GΩ
Output						
R_{OH}	ON Resistance V_H to OUTx	INx = V_S+, I_{OUTx} = -100mA		3.5		Ω
R_{OL}	ON Resistance V_L to OUTx	INx = 0V, I_{OUTx} = +100mA		3		Ω
I_{LEAK+}	Positive Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S+		15		nA
I_{LEAK-}	Negative Output Leakage Current	INx = V_S+, OE = 0V, OUTx = V_S-		-15		nA
POWER SUPPLY						
I_{S+}	V_S+ Supply Current	INx = 0V and V_S+		0.8		mA
I_{S-}	V_S- Supply Current	INx = 0V and V_S+		-0.8		mA
I_H	V_H Supply Current	INx = 0V and V_S+		0.1		µA
I_L	V_L Supply Current	INx = 0V and V_S+		0.1		µA
SWITCHING CHARACTERISTICS						
t_R	Rise Time	INx = 0V to 5V step, C_L = 1nF		11		ns
t_F	Fall Time	INx = 5V to 0V step, C_L = 1nF		12		ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 1nF		1		ns
t_D+	Turn-On Delay Time	INx = 0V to 5V step, C_L = 1nF		11.5		ns
t_D-	Turn-Off Delay Time	INx = 5V to 0V step, C_L = 1nF		13		ns
t_{DD}	t_D+, t_D- Mismatch	C_L = 1nF		1.5		ns
t_{ENABLE}	Enable Delay Time	INx = V_S+, OE = 0V to 5V step, R_L = 1kΩ		12		ns
$t_{DISABLE}$	Disable Delay Time	INx = V_S+, OE = 5V to 0V step, R_L = 1kΩ		27		ns

Typical Performance Curves (Pre-rad)

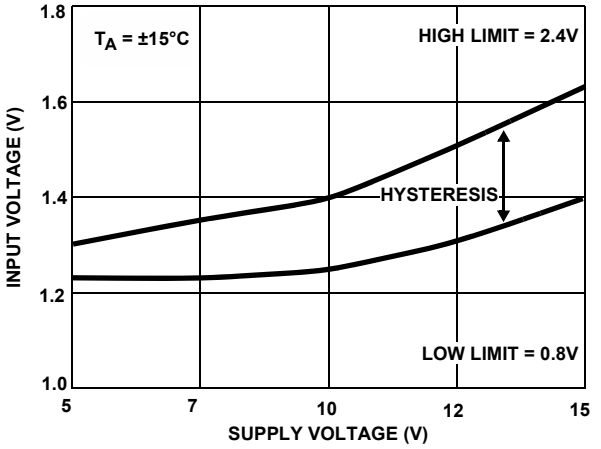


FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE

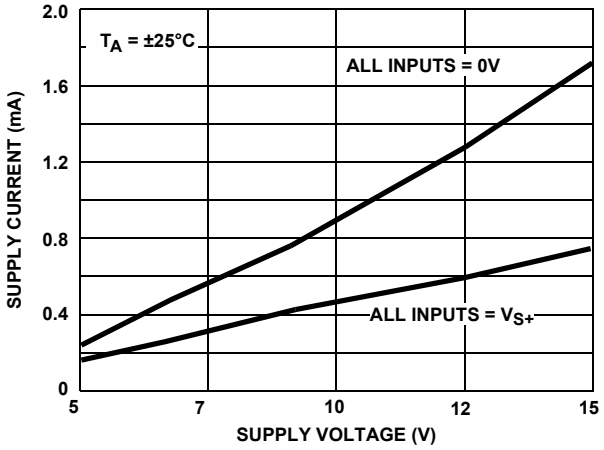


FIGURE 3. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

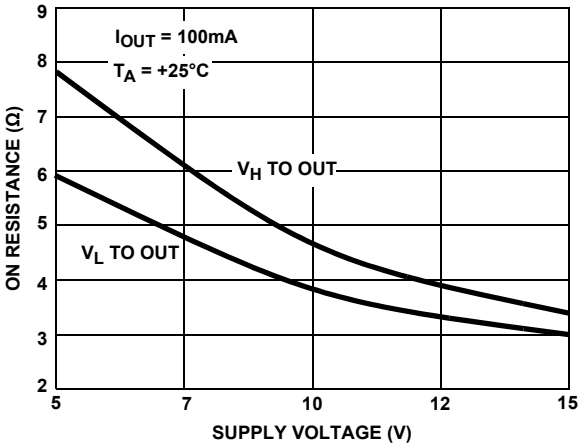


FIGURE 4. ON-RESISTANCE vs SUPPLY VOLTAGE

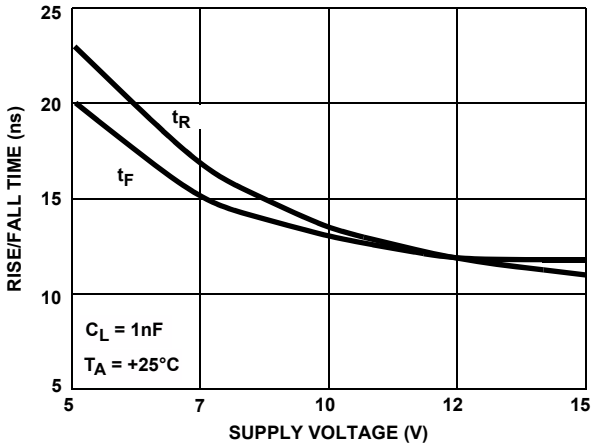


FIGURE 5. RISE/FALL TIME vs SUPPLY VOLTAGE

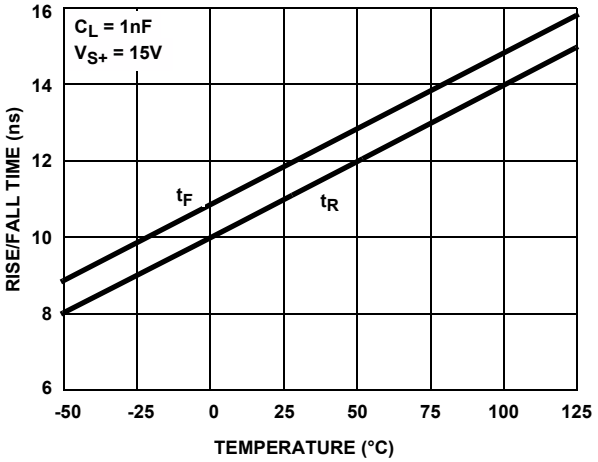


FIGURE 6. RISE/FALL TIME vs TEMPERATURE

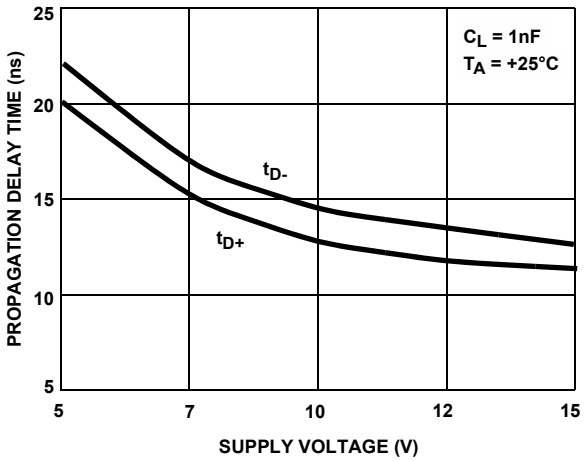


FIGURE 7. PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

Typical Performance Curves (Pre-rad) (Continued)

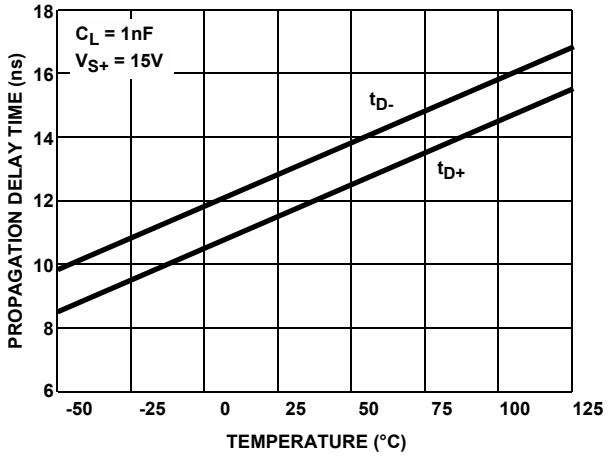


FIGURE 8. PROPAGATION DELAY TIME vs TEMPERATURE

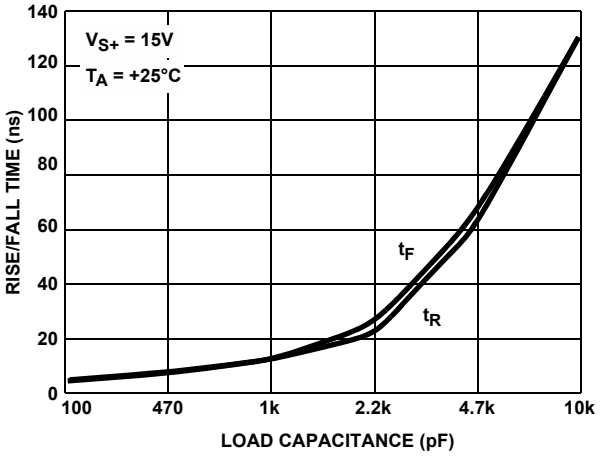


FIGURE 9. RISE/FALL TIME vs LOAD CAPACITANCE

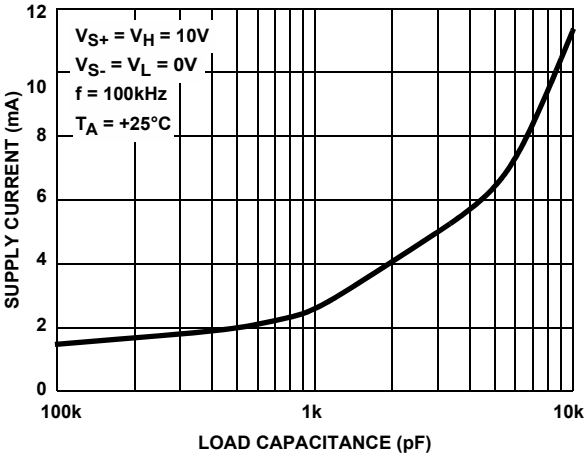


FIGURE 10. SUPPLY CURRENT PER CHANNEL vs LOAD CAPACITANCE

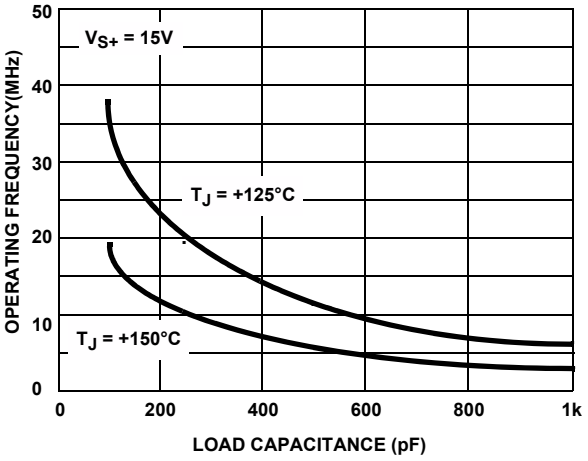
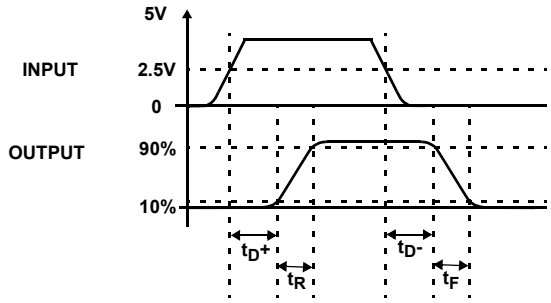


FIGURE 11. OPERATING FREQUENCY vs LOAD CAPACITANCE DERATING CURVES

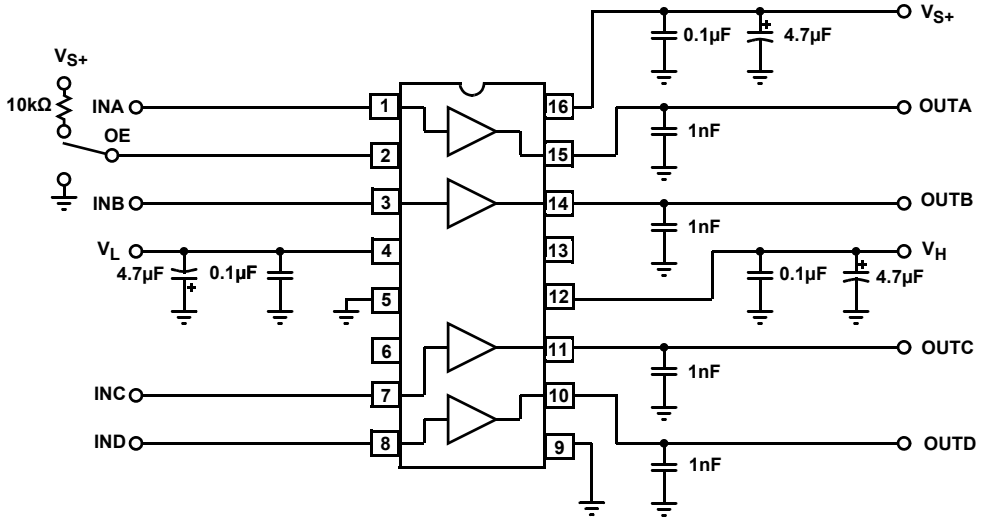
TABLE 1. OPERATING VOLTAGE RANGE

PIN	MIN	MAX
V_S+ to V_S-	4.5V	16.5V
V_S- to GND	0V	0V
V_H	V_S- + 2.5V	V_S+
V_L	V_S-	V_S+
V_H to V_L	0V	16.5V
V_L to V_S-	0V	8V

Timing Diagram



Standard Test Configuration



Application Information

Product Description

The ISL7457SRH is a high performance, high speed quad CMOS driver. Each channel of the ISL7457SRH consists of a single P-channel high-side driver and a single N-Channel low-side driver. These 3.5Ω devices will pull the output (OUTx) to either the high or low voltage, on V_H and V_L respectively, depending on the input logic signal (INx). It should be noted that there is only one set of high and low voltage pins.

A common output enable (OE) pin is available on the ISL7457SRH. When this pin is pulled low, it will put all outputs in a high impedance state.

Supply Voltage Range and Input Compatibility

The ISL7457SRH is designed to operate on nominal 5V to 15V supplies with ±10% tolerance. Table 1 on page 8 shows the specifications for the relationship between the V_S+, V_S-, V_H, V_L, and GND pins. The ISL7457SRH does not contain a true analog switch and therefore V_L should always be less than V_H.

All input pins are compatible with both 3.3V and 5V CMOS signals.

PCB Layout Guidelines

1. A ground plane must be used, preferably located on layer #2 of the PCB.
2. Connect the GND and V_S- pins directly to the ground plane.
3. The V_S+, V_H and V_L pins should be bypassed directly to the ground plane using a low-ESR, 4.7µF solid tantalum capacitor in parallel with a 0.1µF ceramic capacitor. Locate all bypass capacitors as close as possible to the respective pins of the IC.
4. Keep all input and output connections to the IC as short as possible.
5. For high frequency operation above 1MHz, consider use of controlled impedance traces terminated into 50Ω on all inputs and outputs.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the ISL7457SRH drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation, die temperature must be kept below T_{JMAX} (+150°C).

Power dissipation may be calculated as shown in Equation 1:

$$P_D = (V_S \times I_S) + \sum_{1}^{4}[(C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)] \quad \text{(EQ. 1)}$$

where:

P_D is the power dissipated in the device.

V_S is the total power supply to the ISL7457SRH (from V_S+ to V_S-).

I_S is the quiescent supply current.

C_{INT} is the internal load capacitance (80pF max).

f is the operating frequency.

C_L is the load capacitance.

V_{OUT} is the swing on the output (V_H - V_L).

Junction Temperature Calculation

Once the power dissipation for the application is determined, the maximum junction temperature can be calculated as shown in Equation 2:

$$T_{JMAX} = T_{SMAX} + (\theta_{JC} + \theta_{CS}) \times P_D \quad \text{(EQ. 2)}$$

where:

T_{JMAX} is the maximum operating junction temperature (+150°C).

T_{SMAX} is the maximum operating sink temperature of the PCB.

θ_{JC} is the thermal resistance, junction-to-case, of the package.

$\theta_{CS}$is the thermal resistance, case-to-sink, of the PCB

P_D is the power dissipation calculated in Equation 1.

PCB Thermal Management

To minimize the case-to-sink thermal resistance, it is recommended that multiple vias be placed on the top layer of the PCB directly underneath the IC. The vias should be connected to the ground plane, which functions as a heatsink. A gap filler material (i.e. a Sil-Pad or thermally conductive epoxy) may be used to insure good thermal contact between the bottom of the IC and the vias.

Die Characteristics

DIE DIMENSIONS:

2390µm x 2445µm (94.1 mils x 96.3 mils)

Thickness:13.0 mils ±0.5 mil

INTERFACE MATERIALS

Glassivation

Type: PSG and Silicon Nitride

Thickness: 0.5µm ± 0.05µm to 0.7µm ±0.05µm

Top Metallization

Type: AlCuSi (1%/0.5%)

Thickness: 1.0µm ±0.1µm

Substrate:

Type: Silicon

Isolation: Junction

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential:

V_S-

ADDITIONAL INFORMATION

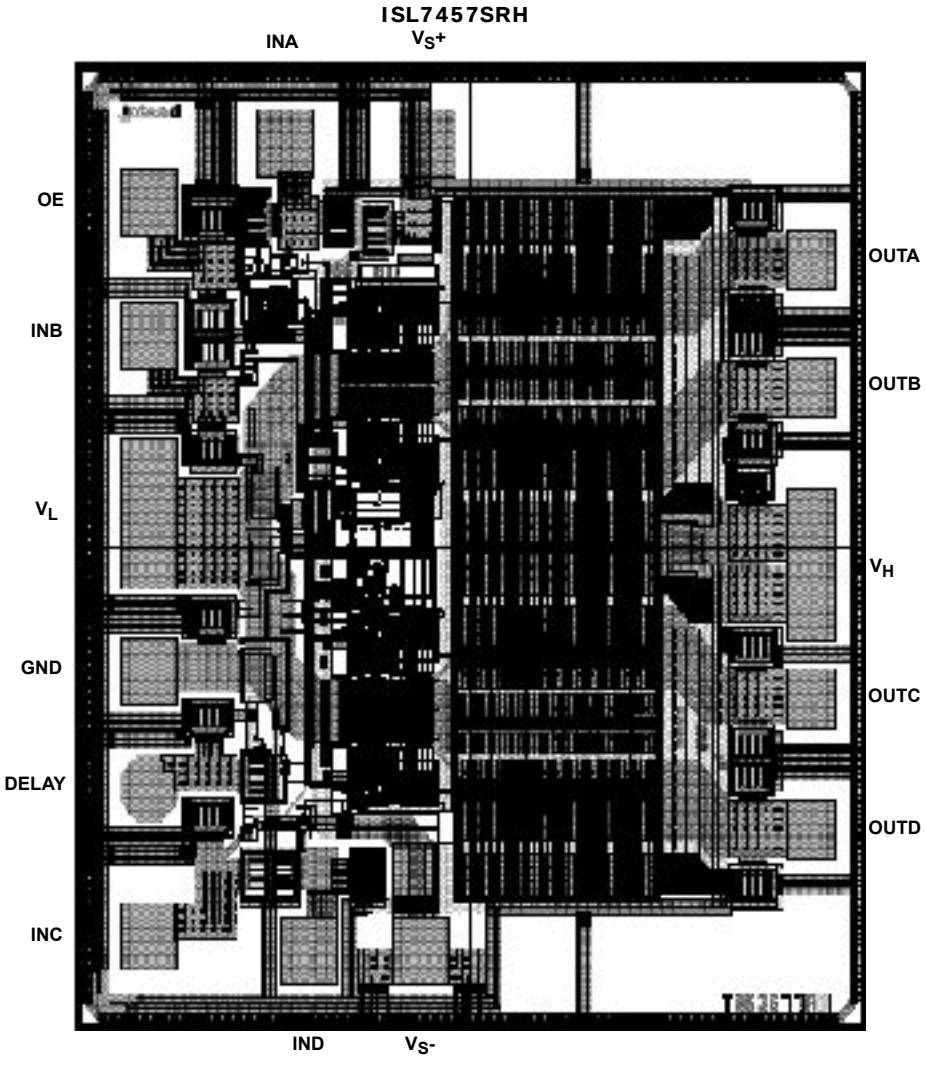
Worst Case Current Density:

$< 2 \times 10^5$ A/cm^2

Transistor Count:

1142

Metallization Mask Layout



Layout Characteristics

Step and Repeat: 2390µm x 2445µm

The DELAY pad is not bonded.

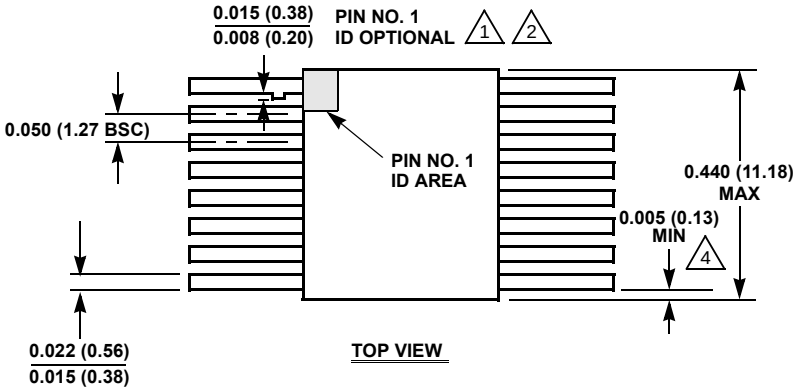
TABLE 1. LAYOUT X-Y COORDINATES

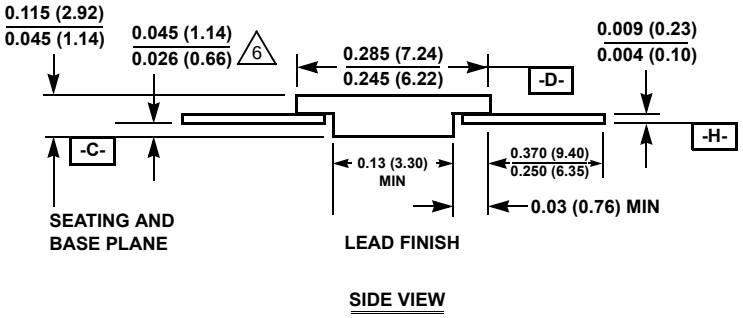
PAD NAME	X (µm)	Y (µm)	DX (µm)	DY (µm)	PROBES PER PAD
IND	675	190	140	140	1
V_{S-}	995	190	140	140	1
OUTD	2118	490	122	133	1
OUTC	2118	795	122	133	1
V_H	2118	1039	122	345	2
	2118	1211			
OUTB	2118	1554	122	133	1
OUTA	2118	1861	122	133	1
V_{S+}	1015	2140	140	140	1
INA	608	2140	140	140	1
OE	213	1993	140	140	1
INB	213	1673	140	140	1
V_L	213	1331	140	345	2
	213	1159			
GND	213	864	140	140	1
DELAY	213	585	140	140	0
INC	213	213	140	140	1

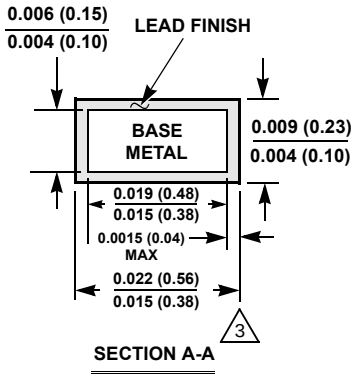
Package Outline Drawing

K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.